Ultra-high Speed and Dual-Channel Data Acquisition Card with 1GSPS Based on PXI Bus

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Abstract: This paper discusses the chief techniques and design principles of an ultra-high speed and dual-channel data acquisition card based on PXI bus, using FPGA (Field Programmable Gate Array) as logic controller cell. The instrument consists of pre-process circuit, A/D converter, SDRAM (Synchronous Dynamic random access memory), and control circuit integrated in FPGA. It can achieve allowing up to 1000MHz real-time sampling rate. The test result indicates that the system works normally and the system design is successful.

Keywords: High-speed data acquisition; Virtual Instrument; PXI Bus; A/D converter; FPGA

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1.Introduction

With the development of science and technology, various data acquisition systems have been applied more and more widely. At the same time, various technical indicators such as sampling rate, resolution, linearity, accuracy, input range, control method, and anti-jamming capability and so on, are also available. Higher and higher requirements are put forward; especially the accuracy and sampling rate are important issues that users and designers pay attention to. As a result, high-speed and ultra-high-speed data acquisition systems have emerged and have been rapidly developed.

The 1GSPS ultra-fast dual-channel data acquisition card is a virtual instrument based on PXI bus. It is developed on the basis of the development of a type of radar intelligent diagnostic system. The acquisition card completes real-time data acquisition with a sampling rate of 1000 MS/s. Simultaneously, the card has 128 MB of SDRAM and can record data in real time at 100 MHz/s. It uses PXI bus and computer interface, through the software driver to read data into the memory in the form of data blocks to complete the data processing and display functions. The acquisition card has the characteristics of strong data throughput, good real-time performance, compact structure, low power consumption, high reliability and strong functions.

2.Overall Structure of the Acquisition Card

The overall structure of the ultra-high-speed dual-channel data acquisition card is shown in Figure 1. It consists of a preprocessing circuit, A/D conversion circuit, SDRAM, high-frequency clock and timing generation circuit, and a Nios II CPU and PXI interface controller integrated in the FPGA chip. , SDRAM controller composition. The range of the amplitude of the input signal may vary greatly, and the function of the preprocessing circuit is to amplify or attenuate the conditioning to adapt it to the input requirements of the A/D converter. The A/D conversion circuit is responsible for converting the analog quantity into a digital quantity, and the converted digital quantity signal is sequentially written into the SDRAM under the control of the SDRAM controller. The two signals of the acquisition card share a set of A/D conversion circuits, so a high-speed dual selector is added in front of the A/D conversion circuit, and the data acquisition of the two signals is completed through fast switching. The PXI interface controller here is implemented by embedding the PXI soft core (IP Core) into the FPGA chip, conforming to the PXI local bus specification, enabling complete PXI interface functions and achieving basic transfer requirements. The entire acquisition card is in an orderly manner under the control of a highly stable clock generated by a high-frequency clock generator.

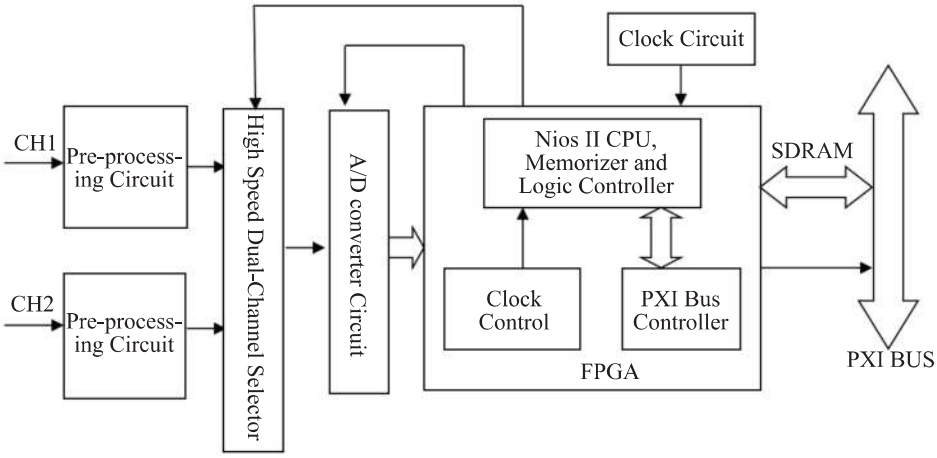

Figure 1. The Overall Structure of Acquisition Card

3. Circuit Design and Realization of the Acquisition Card

3.1 Pre-processing Circuit and A/D Converter

The core of the data acquisition circuit is the A/D converter, while the input signal range allowed by the high-speed A/D chip is generally fixed (for example, -0.5 to +0.5 V). The preprocessing circuit consists of a resistance-capacitance attenuation network, an impedance transform, and a master. Amplification, offset adjustment and drive amplification are shown in Fig. 2. Its function is to attenuate or amplify the input signal to the allowable range of the A/D chip. Here the attenuation network is completed by the FPGA control relay. At the same time, increase the input impedance to reduce the impact on the signal. The main amplifier uses the AD8056 wideband operational amplifier. The main characteristic of this chip is the 300MHz bandwidth (-3dB Bandwidth, G=+1). The resistance-capacitance matching network in the actual circuit also includes an AD8056, which is mainly used as a follower to perform isolation. The driving amplifier circuit uses the AD8138 from AD Company as the input driver and signal level converter of the A/D converter. The dc shift level is output by the DAC and is programmed by the computer.

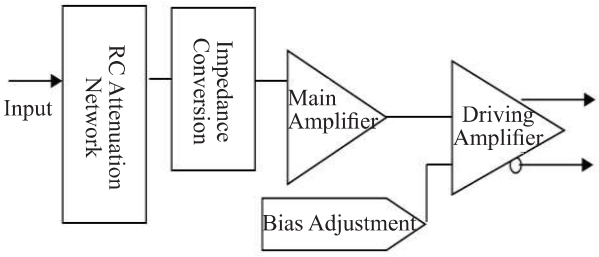

Figure 2. Pre-process Circuit Structure

The A/D converter completes the analog/digital conversion of the electrical signal. In order to achieve a sampling rate of 1000 MS/S, the AD9054A chip with the highest sampling rate of 135 MS/S is used here. Its accuracy is 8bit and the analog input bandwidth is 2.2GHz. The AD9054A is designed to integrate many peripheral circuits such as sample and hold and reference voltage circuits into the chip, which greatly facilitates the use of the user. The outputs of the AD9054A are all based on PECL logic, which provides three alternative operating modes. One AD9054A contains two PECL outputs, each with an input amplitude range of 1 V peak-to-peak (p-p), a single 3.0 V supply (2.7 V to 3.6 V), and an output data format of two's complement format or offset binary (offset) Format[1]. Here, eight AD9054A chips with a sampling rate of 125 MS/S are used to form a sampling circuit of 1000 MS/S. The parallel A/D sampling schematic is shown in Figure 3.

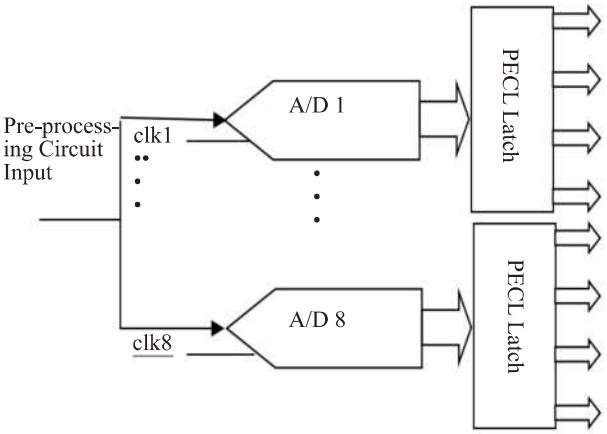

Figure 3. A/D Acquisition Diagram

3.2 Circuit Design and Realization of the High-frequency Clock and Timing Sequence Generation

Data acquisition card using eight AD9054A, a total of eight A / D converters, sampling clock sent to each chan-

nel is 125MHz and a phase difference of 45° making them at the same time on the same input signal digital sampling, splicing together to reach 1000MS / S The sampling rate. One of the key technologies of this acquisition card is the high-frequency clock and timing generation circuit design. The sampling circuit clock (ENCODE) signal is PECL level. For high-speed clock circuits, aperture jitter is a very important indicator for selecting a clock source. Jitter refers to the clock edge itself is not stable, shaking in a certain range, the shaking of the clock edge will bring the uncertainty of the sampling point, the higher the frequency of the sampled signal is greater error[2]. After investigation, the FPGA internal phase-locked loop is used to double the input clock to generate an A/D sampling clock. The design uses the altpll (Phase-Locked Loop) Megafunction in the Quartus II library for design. Finally, the A/D sampling clock is output via the pins at equal phase intervals. The timing is shown in Figure 4, with clk0 to clk7 at 45° hase angles.

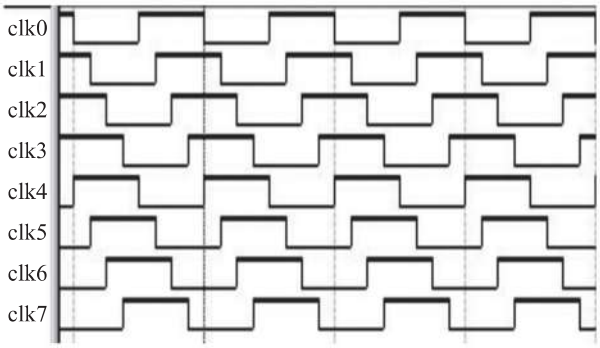

Figure 4. Sampling Clock Timing Diagram

3.3 SDRAM Controller

SDRAM is characterized by its large storage capacity and high speed, and is widely used in computer memory modules. The role of the SDRAM controller is to correctly write the 8-channel data output from the A/D chip into the memory on the module at a rate of 100 MHz/s. It is also responsible for correctly reading the stored data and sending it to the PXI controller, and then sent to computer memory which is also responsible for SDRAM refresh. The SDRAM controller designed by the acquisition card is based on the SDRAM Controller (IP core) of Altera Corporation and is modified by the specific application of the project[3]. Its internal structure includes central control module, initialization module, refresh module, address generation module and data block management 5 modules. The central control module controls various operating modes of the SDRAM, and its value can be configured through the interface. It is also responsible for arbitrating the user's read and writes request signals, initialization requests, and refreshes requests. The result of arbitration produces various operating instructions for SDRAM. The address generation module and the data block management module are respectively responsible for addressing the storage unit of the SDRAM and the input and output management of the data block. The SDRAM controller in the actual circuit is programmed in Verilog-HDL on the FPGA chip, and a functional simulation is done using the ModelSim simulation tool[4]. In addition, Figure 5 shows the block diagram of its internal structure.

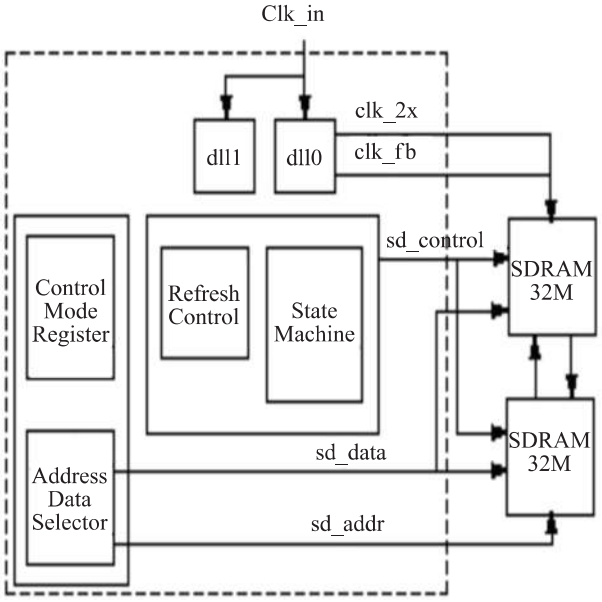

Figure 5. The Internal Structure of SDRAM Controller

3.4 Design of the Trigger Channel

The trigger circuit is an important functional circuit of the signal acquisition system. Its basic function is to provide a stable trigger phase point, which is used as the time reference zero point of the horizontal scan time base, so that the waveform is displayed stably on the display screen. The acquisition card is designed to implement a period of the trigger pulse signal associated with the measured signal to control the ADC data acquisition.

The core component of the trigger circuit is a high-speed level comparator. The AD96685 chip is used in this acquisition card. Trigger circuit shown in Figure 6. The Trig Level signal superposes the comparison level of the low-frequency component of the source signal, Ref is the reference potential, and the Trig Source signal is the source signal that is triggered. By changing the level of the Trig Level signal, the trigger level is adjusted. A pair of ECL differential clocks, TrigP and TrigNP, are output after comparison through the AD96685, and then convert-

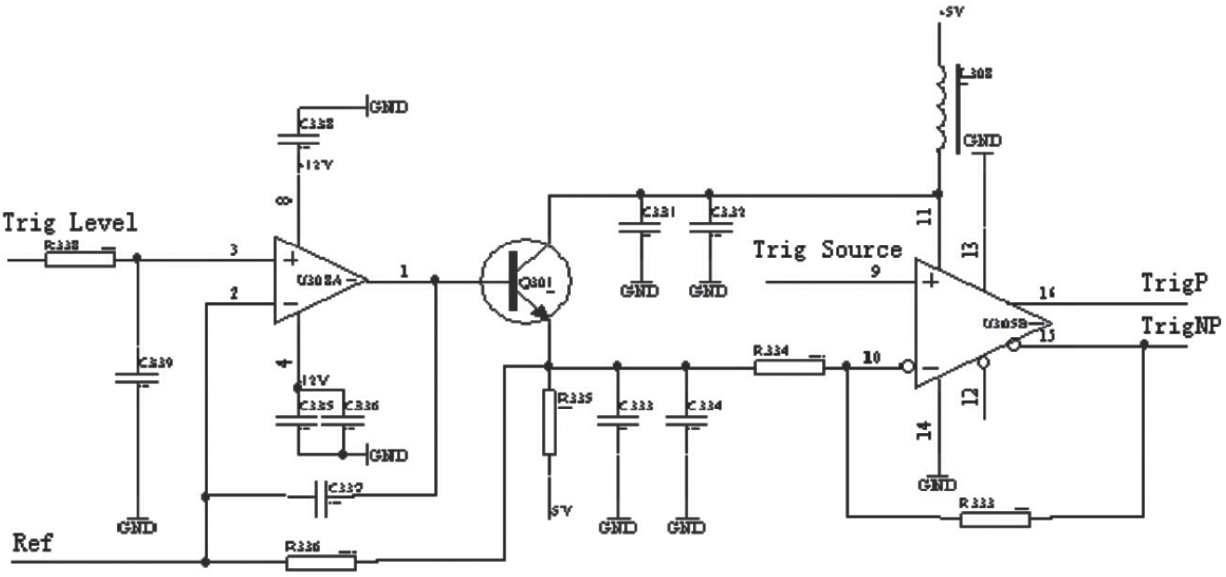

Figure 6. Trigger Circuit

ed into the trigger in the FPGA after level conversion.

3.5 Interface Circuit of PXI Bus

PXI (PCI Extension for Instrumentation) is an extension of PCI in the instrument field. It develops the PCI bus technology defined in the Compact PCI specification into mechanical, electrical, and software specifications suitable for applications in test, measurement, and data acquisition environments, resulting in new virtual Instrumentation architecture[5]. In order to develop an autonomous PXI interface to save resources and enhance system flexibility, this acquisition card uses SOPC technology, fully utilizes FPGA to implement the design of PXI interface, and optimizes the design of functional interfaces according to the needs. Logic and PXI interface logic are integrated into the same chip, which fully saves the system's logic resources. The FPGA selected by the capture card is EP3C16Q240C8N chip of Altera Company, he has 15408 logic units, embedded RAM of 504Kb, four internal PLLs and 56 multipliers. The chip's I/O supports a large number of different single-ended interfaces and differential data interfaces, and provides users with 160 I/O ports, which can fully meet the requirements of PXI bus operations on resources.

4. Conclusion

This paper mainly introduces a 1GSPS super high-speed dual-channel data acquisition card system based on PXI bus. The acquisition card has been successfully used in a type of radar intelligent diagnosis system. The actual test results show that the system is working properly and all the indicators are in line with the expected values. The acquisition card uses FPGA chip and SOPC (system-on-a-programmable-chip) technology, which greatly simplifies the circuit design and reduces costs. It can be used in radar, communications, measurement, multimedia and other fields, and has broad application prospects.

The author of this paper innovated: proposed multi-body cross-parallel high-speed data acquisition card architecture based on SOPC, and realized the goal of 1GSPS high-speed data acquisition with low-speed, low-cost analog-to-digital conversion devices. The in-depth study of this technology will be of great significance in promoting the rapid development of China's new digital information processing technology, and will play a positive role in improving the level of informatization in communications, measurement and control, meteorology, and military equipment.

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