

Research and Development on an Embedded Digital Storage Oscilloscope Based on PXA 270

Pengyun Zhang^{1*} Guonan Feng² Zhiqiang He³

School of Information and Technology, Hebei University of Economics and Business, Shijiazhuang, Hebei, 050061, China

Abstract: This paper discusses the chief techniques and design principles of an embedded digital storage oscilloscope based on PXA 270, using FPGA as logic controller cell. The data acquisition partition consists of pre-process circuit, A/D converter, on-board memories, and control circuit integrated in FPGA. In the PB and EVC development environment, developers realized the part of embedded software. Actual test showed that the highest real-time sampling rate of the oscilloscope is up to 1GHz/s, which has achieved the desired design requirements.

Keywords: High-speed data acquisition; Embedded; PXA 270; A/D converter; FPGA

***Corresponding Author:** Pengyun Zhang, Hebei University of Economics and Business, No. 47, Xuefu Road, Xinhua District, Shijiazhuang, Hebei, 050061, China. E-mail: 287057031@qq.com.

Fund Project: Hebei Province Applied Basic Research Project (Project No.: 10963529D)

DOI: <http://dx.doi.org/10.26549/met.v2i2.851>

1. Introduction

With the development of science and technology, traditional oscilloscopes have been unable to meet the needs of users for equipment information applications, and put forward higher and higher requirements for the performance of test instruments. At the beginning of the 21st century, with the continuous innovation and development of microelectronics technology, embedded systems, as an important field of computer applications, have the characteristics of good real-time performance, high performance, low power consumption, compact structure and object-oriented, which leads to rapid development. The embedded digital storage oscilloscope combines embedded technology and oscilloscope to develop a new

intelligent measuring instrument with data exchange, multi-parameter automatic analysis, and information synthesis and judgment control.

The embedded digital storage oscilloscope developed by this project uses Intel XScale PXA 270 as the embedded CPU, and the tailored WinCE is the embedded operating system. Real-time data acquisition can be completed at a sampling rate of 1000MS/s, while the card has 128MB synchronous dynamic random access memory (SDRAM), which can record data in real time at 100MHz/s. It uses a data interface bus to connect to the embedded CPU, and the data is read into the memory as a data block by the software driver, and the data processing and display functions are completed by the application developed by the EVC.

2. System Overview

The overall structure of the digital storage oscilloscope is shown in Figure 1. It consists of hardware and embedded software. The hardware is divided into embedded CPU PXA270 main control board and data acquisition board. The main control board provides an environment for the entire system operation and management, and realizes the control of peripherals such as keyboard, mouse and LCD screen. The data acquisition board is composed of a pre-processing circuit, an A/D conversion circuit, an SDRAM, a high frequency clock and timing generation circuit, and a Nios II CPU, a bus interface controller, and an SDRAM controller integrated in the FPGA chip. For the amplitude range of the input signal can vary greatly, the role of the pre-processing circuit is to amplify or attenuate it to fit the input requirements of the A/D converter. The A/D conversion circuit is responsible for converting the analog quantity into a digital quantity, and the converted digital quantity signal is sequentially written into the SDRAM under the control of the SDRAM controller.

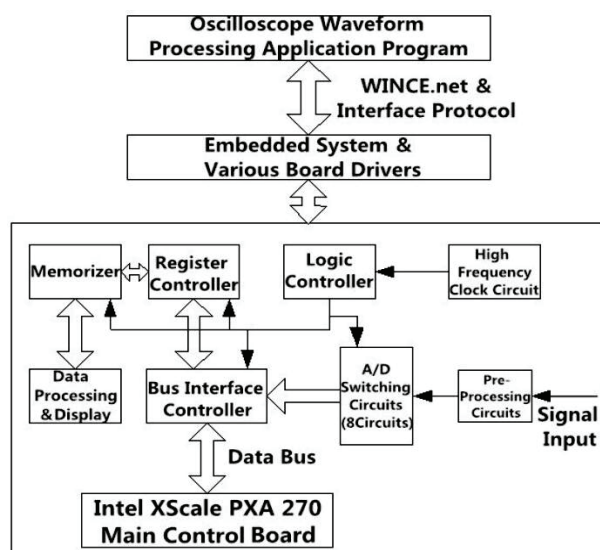


Figure 1. The Overall Structure of Oscilloscope

And through the data interface controller realized by the FPGA chip, the data transmission is completed. The entire capture card is ordered for operation under a highly stable clock, which is generated by a high frequency clock generator. Embedded software is divided into a kernel subsystem and an application subsystem. The development of the kernel subsystem is designed to implement WinCE system tailoring, BootLoader porting, OAL design and driver programming. The application subsystem design implements functions such as data acquisition, data processing, data display, and system setup. The oscilloscope CPU has a frequency of up to 520MHz and a

real-time sampling rate of up to 1GSPS.

3. Hardware Circuit Design

3.1 Main Control Board Circuit

The design uses PXA270 as the embedded CPU. The PXA270 is an XScale-based processor developed by Intel Corporation. The core uses ARMv5TE and has many peripheral controllers. Built-in Intel's wireless MMX technology can significantly improve multimedia performance. In addition, the PXA270 also includes Intel's SpeedStep technology, which can dynamically adjust the CPU performance as needed, realizing low power consumption and high performance. Like other XScale processors, it supports multiple embedded operating systems such as Linux, Windows, WinCE, Java, etc.^[1] The main control board also uses Samsung K4S561632 as the memory chip, and Intel's NOR FLASH 28F128 flash chip is used to solidify the embedded operating system. Complete the USB interface with CY7C67300, design the network interface with CS8900, and design the audio interface with IL4297. The digital signal after A/D converter is written into the buffer memory under the control of the controller. The data is displayed on the LCD or stored in the SD card through the local bus under the control of the CPU for verification. The functional structure diagram is as follows. (Figure 2)

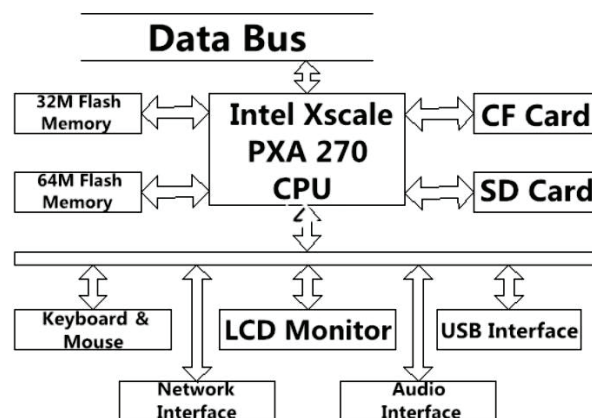


Figure 2. The Structure of Main Control Board

3.2 Data Acquisition Circuit

The core of the data acquisition circuit is the A/D converter. Considering the sampling rate, design cost, power consumption and transmission format, the 8-channel AD9054A chip is used here to complete the design requirements of 1GSPS through parallel alternate acquisition technology. The working principle is as follows. (Figure 3) The pre-processing circuit consists of a resistor-capacitor attenuation network, impedance transformation, main amplification, offset adjustment, and drive am-

plification. Its function is to attenuate or amplify the input signal to the allowable range of the A/D chip.^[2] The signal is simultaneously sent to eight parallel channels in the analog-to-digital conversion array and sampled under the control of the clock signal. The clock signal CLK is controlled by a high-precision FPGA internal phase-locked loop clock circuit. The clock phase difference is strictly guaranteed to be $360/8=45^\circ$, so that each ADC of the system is sampled by a signal whose frequency is reduced by 8 times. This enables low-speed chips to achieve high sampling rate design goals. Since the control signal is a serial bus structure, the 8-way parallel data is outputted at a high speed after parallel-serial conversion. Then, the data is serially synthesized and processed to achieve high-speed analog signal reproduction.

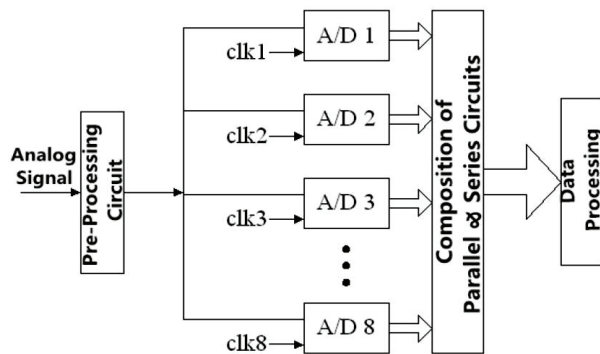


Figure 3. Data acquisition Schematic

The AD9054A chip has a maximum sampling rate of 135MS/S, and its precision is 8bit. The analog input bandwidth is 2.2GHz. Many peripheral circuits such as sample-and-hold and reference voltage circuits are integrated into the chip, which greatly facilitates users' usage. The output of the AD9054A is based on PECL logic and offers three optional operating modes. The AD9054A has an input amplitude range of 1.0 V peak-to-peak (p-p), a 3.0 V single-voltage supply (2.7 V to 3.6 V), and an output data format of two's complement format or offset binary format. And the area is only $7 * 7\text{mm}^2$, each piece consumes only 90mW.^[3] The AD9054A has an output data bit width of 8 bits and a full-scale input voltage range of 1.024V, so its minimum voltage resolution is $1.024\text{V}/28=4.0\text{mV}$. The design uses eight AD9054A chips with a sampling rate of 125MS/S to form a sampling circuit of 1000MS/S.

3.3 Clock Circuit

The data acquisition circuit uses 8 AD9054A, a total of eight A/D converters, and the sampling clocks sent to each channel are 125MHz and the phase difference is 45 degrees, so that they can digitally sample the same input signal at the same time, and can achieve the sampling rate

of 1000MS/S by splicing together. One of the key technologies of this acquisition circuit is the high frequency clock and timing generation circuit design. The sampling circuit clock (ENCODE) signal is at the PECL level. For high-speed clock circuits, aperture jitter is a very important indicator of the choice of clock source. Jitter means that the clock edge itself is unstable and sways within a certain range. The sloshing of the clock edge will bring uncertainty to the sampling point. The higher the frequency of the sampled signal, the greater the error is. After investigation, ALTERA's EP3C10F256 was selected as the FPGA of the system. The chip integrates two phase-locked loops and 10 clock lines, which fully meets the design requirements of the system for high-frequency clock circuits.^[4] 182 user I/O ports and 423936 bits of storage resources can fully meet the data storage and transmission requirements of 8-way AD. Here, the FPGA internal phase-locked loop is used to multiply the input clock to generate an A/D sampling clock. The design uses the altpll (Phase-Locked Loop) Megafuction in the Quartus II library for design. Finally, the A/D sampling clock with equal phase spacing is output via the pin. The timing is shown in Figure 4. The clk0~clk7 are separated by a phase angle of 45° .

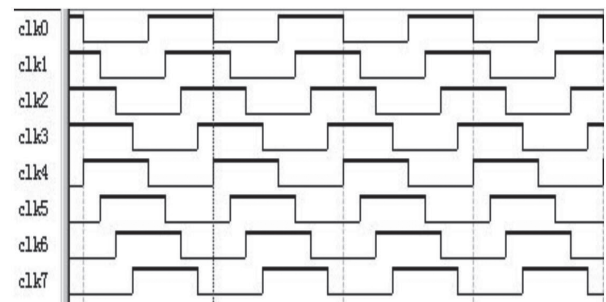


Figure 4. Sampling Clock Timing Diagram

3.4 Trigger Circuit

The trigger circuit is an important function circuit of the signal acquisition system. Its basic function is to provide a stable trigger phase point, which is used as the time reference zero point of the horizontal scanning time base, so that the waveform is stably displayed on the display screen. The acquisition circuit design realizes a trigger pulse signal related to the measured signal in one cycle, and controls the ADC data acquisition.

The core component of the trigger circuit is a high-speed level comparator. The AD96685 chip is used in this acquisition circuit. The trigger circuit is shown in Figure 5. The Trig Level signal is the comparison level at which the low frequency component of the source signal is superimposed, Ref is the reference potential, and the Trig Source signal is the source signal that is triggered. The adjustment

of the trigger level is achieved by changing the level value of the Trig Level signal. After the AD96685 compares and shapes, it outputs a pair of ECL differential clocks, TrigP and TrigNP, and then is level-converted and sent to the trigger in the FPGA.

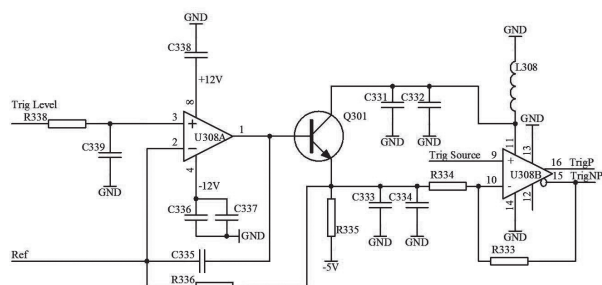


Figure5. Trigger Circuit

4. Embedded Software Design

4.1 Kernel Subsystem

Under the Platform Builder development environment provided by Microsoft to Windows CE.NET developers, the design, creation, compilation, testing and debugging of embedded operating systems can be completed. Customize the complete operating system through PB according to the embedded hardware selected, Which are composed of BSP (Mainboard Support Package), Core OS Services (Core OS Services), Object Storage and Registry, Multimedia Technology, Communication Services and Network Components.^[5] The BSP is a software package that includes drivers for the launcher, OEM Adaptation Layer (OAL), standard development board (SDB), and related hardware devices.

1) BootLoader is a separate program code, usually stored in the non-volatile storage medium read-only memory or flash memory of the target platform. This program is mainly used to develop platform hardware startup and download NK.Bin program, and play a monitoring role.

2) OAL is the code layer between the Windows CE kernel and the target device hardware to simplify communication between the operating system and hardware devices, interrupt handling, timers, power management, bus management, and general-purpose IO control.

3) Windows CE driver is an abstract physical device or virtual device functional software that manages the operation of abstract or virtual devices, in the form of user-mode DLLs (dynamic link files). The driver in the system design consists of a local device driver for data acquisition and a stream device driver such as a network card or USB.

Next, through the compilation of Sysgen, Feature Build, Release Copy and Make Image 4 stages, the em-

bedded operating system image file NK.bin is completed. After downloading NK.bin to the target machine, the WinCE system can be started, and then select Build SDK under the PB platform menu. After the compilation is completed, select Configure SDK, and PB will automatically generate an SDK (software development kit) installation file. Install the installation file on the computer, then open EVC (Microsoft eMbedded Visual C++), find the SDK platform just installed in the platform selection, and then develop the application software based on the SDK platform.

4.2 Application Subsystem

The overall structure design of the oscilloscope application software subsystem is mainly composed of four modules: data acquisition, data processing, data display and system setting.

1) Data acquisition module design mainly includes: data acquisition control, time base control, attenuation control and trigger control.

2) The data processing module design mainly includes: waveform calculation and measurement of waveform attribute values.

3) The data display module design mainly includes: waveform display control and measurement information display control.

4) System setting module design mainly includes: storage settings and system settings.

In order to effectively improve the system resource utilization, the data acquisition and data display parts are separately processed in separate threads. Through the event object to control the cooperation between threads, to achieve their direct synchronization operation, effectively solve the problem of accessing shared resource conflicts, so that system resources can be better utilized. The application software Scope.exe file is stored in the SD card. Through the internal settings, the oscilloscope application is directly accessed after the system is started.

In the actual measurement process, we hope that the data displayed shows as much information as possible. However, due to the slow data processing speed of digital oscilloscopes, the way to collect waveform segments is adopted in the design, so that it is easy to miss some small key information. Therefore, we use the afterglow technology in the design of the data display module, which effectively improves the capture rate of data acquisition. The realization of the afterglow effect is one of the core technologies of the software system, which realizes the display of the waveform track, and can set the afterglow time according to the needs of different users to achieve the desired effect. Effectively improve the waveform data analysis capabilities. The waveform display with the af-

terglow effect and without the afterglow effect is shown in Figures 6(a) and 6(b).

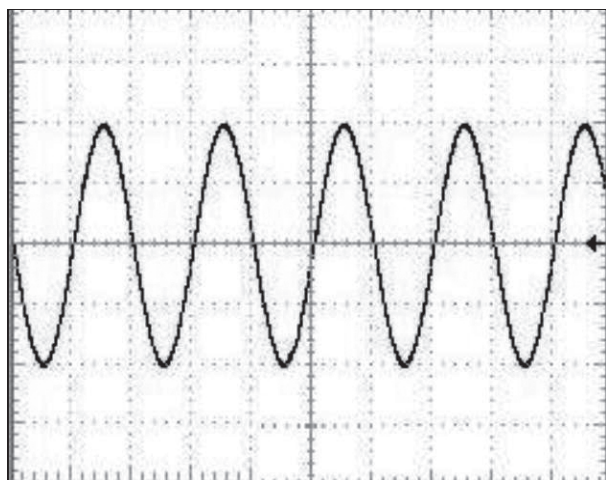


Figure 6(a). Without Afterglow Effects

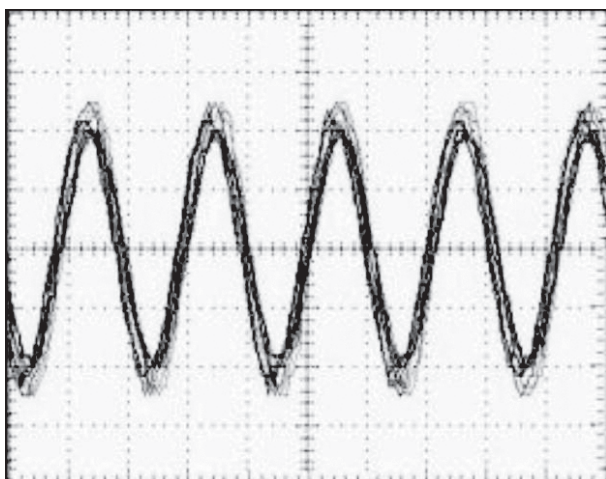


Figure 6(b). With Afterglow Effects

5. Conclusion

This paper mainly introduces some key technologies in the development of an embedded digital storage oscillo-

scope based on PXA 270. The digital storage oscilloscope has successfully developed a prototype, as shown in Figure 7. The oscilloscope uses an embedded CPU, FPGA chip and SOPC technology, which greatly simplifies the circuit design and reduces the cost. The actual test results show that the system works normally, and the indicators are consistent with the expected values. It can be used in radar, communication, measurement and other fields, and has broad application prospects.

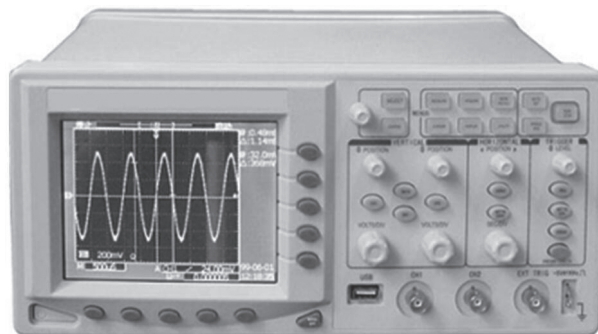


Figure 7. Product Prototype

References

- [1] Jinli Wang, Wanxin Su. Embedded System Design Based on PXA270[J]. Microcomputer Information.2008, 4(2):11-12. (DOI: 10.3969/j.issn.1008-0570.2008.11.005)
- [2] Zhiqiang He, Wenxian Zeng, Shijian Xue. 400MSPS Embedded Virtual Digital Storage Oscilloscope[J].Journal of Scientific Instrument. 2005, 26(9):949-952. (DOI:10.3321/j.issn:0254-3087.2005.09.016)
- [3] Electronic Catalog of Analog Inc. AD9054 Chip Parameters. pdf[EB/OL]http://www.analog.com.1999. (in Chinese)
- [4] Altera.EP3C10F256 Data Electronic Literature. pdf[EB/OL]http://www.altera.com.2009. (in Chinese)
- [5] Wenxian Zeng. Software System Design of 1GSPS Embedded Digital Phosphor Oscilloscope[J]. PACCS 2009: 240-243. (in Chinese)